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Design-for-Test Optimization for Low-Power Semiconductor Devices: A Survey

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***Abstract*—A big design challenge for semiconductor devices is power consumption during testing, since these devices are getting smaller while getting more complicated and having more integration density. If the tests are to be economical, scalable, and dependable without sacrificing performance or adding extra system costs, it need to optimize the Design-for-Test for low power consumption. This survey provides an in-depth analysis of important low-power DFT approaches, such as clock gating, scan chain reordering, Built-In Self-Test (BIST), and test data compression, with the goal of minimizing static and dynamic power consumption during testing. In order to manage switching activity, leakage currents, and enable complicated System-on-Chip (SoC) architectures, power-aware DFT is crucial. The evolution of BIST architectures and the use of low-power test controllers in portable and high-performance systems are discussed in detail. Additionally, the impact of semiconductor scaling, multi-voltage domains, and advanced packaging technologies on test strategies is explored. Emerging trends such as AI-driven test generation and adaptive power control offer promising directions for sustainable and intelligent test solutions. These strategies not only enhance test efficiency and coverage but also contribute to reducing thermal stress, extending device lifespan, and supporting green design initiatives in modern semiconductor development.**

***Keywords*—Low-power design, Design-for-Test (DFT), BIST, power-aware testing, semiconductor devices.**

I. INTRODUCTION

The heart of any power electronic system is a power semiconductor system. Aside from their widespread use in renewable energy systems, electric vehicles, machine drives, and industrial equipment, power semiconductor devices play an essential role in power conversion systems [1]. Having the power electronics system work reliably is crucial for these applications. Looking at it through an engineering lens, reliability is the likelihood that a system or component will perform as expected for a specific period of time and under a given set of conditions, without failing. Earlier it was mentioned that power semiconductor devices play an essential function in the power electronics system and thereby significantly impact the system's reliability.

Power semiconductor devices are exposed to thermal stressors caused by power cycling, which pose the greatest threat to their reliability, according to an industry survey [2]. As a result, power cycling tests (PCT) are one of the most vital and effective methods for assessing the reliability of power semiconductor devices, examining their failure mechanisms, testing new packaging materials and designs, and developing lifetime models to aid in reliability design under mission profiles.

Design for Test (DFT) has become an inescapable discipline in semiconductor engineering, owing to the increased complexity and scale of integrated circuits (ICs) with billions of transistors [3]. In HPC and GPU contexts, DFT lies at the cutting edge of the functional correctness of chips, fault tolerance, and production viability for chips that operate at the edge of speed, power, and concurrency [4]. Tests of these modern chips (which commonly appear in data centers, AI training, and rendering engines) require robust test strategies that can reveal subtle defects without sacrificing their time to market and yield targets.

A circuit's power consumption increases during testing compared to normal operation, which is why test or DFT engineers primarily focus on this aspect. As Zorian demonstrated, the test power need not be half of what the usual mode power consumption is. The rise in electricity consumption can be attributed to multiple factors [5]. First, the switching activity of all nodes is typically many times higher during test mode than during regular operation [6]. This is because test efficiency correlates with toggling rate. Secondly, test engineers may cause unnecessary power and energy loss by utilizing parallel testing in systems on a chip (SoC) to shorten the duration of the test application. Thirdly, while performing tests, the DFT circuitry that was built to simplify them may be heavily utilized, even though it sits idle during regular operation. The fourth point is that there is a strong relationship between the functional input vectors that are applied to the same circuit in system mode.

Low-Power Internal Self-Evaluation One DFT technique is logic built-in self-test (BIST), which involves using a section of the CUT to test itself. Since it offers the capability to self-assess, reasoning Many applications rely on BIST, especially Low Power The goal of logic BIST testing is to achieve high fault coverage, however a big problem is that the power consumption during BIST can go over the chip's or package's power rating [7]. The chip can get hot from an increase in average power, and noise-related faults can occur from a rise in peak power. Several low powers are covered in it. Building Information Models and Techniques for Energy Saving.

A. *Structure of the Paper*

The paper is organized as follows and a brief explanation of DFT fundamentals is included in section II. Section III goes through ML paradigms of DFT. Section IV implements ML to the detection of defect using comparison between traditional and deep learning. Section V looks at low power testing strategies. Section VI finishes with thoughts and plans on how to have effective, scalable DFT.

II. Low Power Issues in Semiconductor Testing

The power used in testing semiconductors is also a matter of serious concern, especially in the context of low-power devices. Unnecessary switching activity due to test patterns tends to increase dynamic power, which may exceed the usual running power, and could potentially damage the device [8]. This proves to be a particular issue in deep submicron technologies, which have higher leakage currents, thereby wasting static power as well. There is also a yield and reliability penalty due to high test power, including IR-drop, overheating, and false failures [9]. Control of test power is therefore critical to the integrity of devices, as it prolongs battery life in portable devices and helps attain thermal design limits. To overcome these challenges associated with power that do not interfere with test coverage, design-for-test (DFT) strategies like scan chain segmentation, clock gating, and test controllers performed at low power have been developed.

A. *Low-Power Test Data Compression*

In general, low shift-power testing methods can be put into two groups: ATPG-based solutions and DFT-based solutions. ATPG-based methods, like test vector reordering, adjacent filling, and X-filling ATPG, try to reduce the number of times test patterns have to move while tests are being generated.

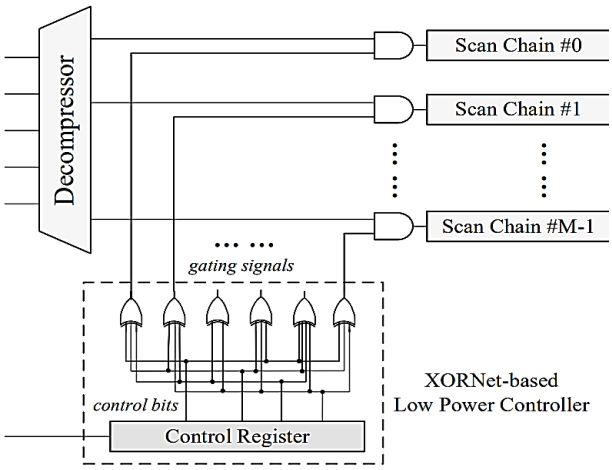

Fig. 1. The XOR Net-based Low Power Test Compression Architecture

Low-power test techniques based on density-functional theory (DFT) utilize hardware features including clock gating, test point insertion, adaptive power scaling, scan chain partitioning, and low-power controllers to decrease switching activity during testing. Among these, low-power controllers are widely used due to their compatibility with test compression [10]. Typically implemented using LFSR- or XOR Net-based encoders, they generate gating signals for scan chains to reduce test power by combining them with decompressed scan data. A representative XOR Net-based low-power controller is shown in Figure 1.

B. *Importance of Low-Power Applications using Semiconductor Devices*

The growing need for efficient and powerful electronic systems has shifted semiconductor research and development towards low-power design. Recent years have seen tremendous progress, made possible by the idea of introducing integrated circuits in 1958, which facilitated the creation of sophisticated electronic components [11]. In order to fulfil the specifications of design engineers for rapid and low power, the components of semiconductor devices are going through major changes, particularly in size. Scaling gadget measurements are commonly based on Moore's law. Since 1970, the smallest element sizes of MOSFET devices have decreased, allowing for an increase in the total number of semiconductors in a single integrated circuit (IC), as illustrated in Figure 2 below:

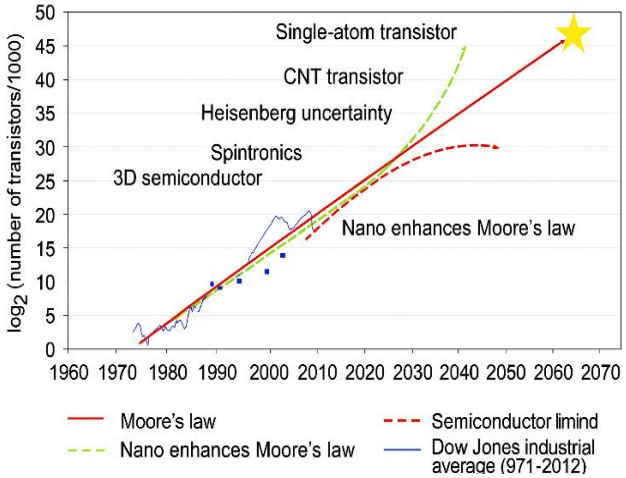

Fig. 2. Moore's Chart

C. *Design Challenges and Reliability Concerns in Testing Power Semiconductors*

Power semiconductor devices, packaged as discrete components or modules, are the fundamental building blocks for power electronic applications [12]. These packages provide electrical connections, thermal management, and insulation. As shown in Figure 3, a legacy power module comprises multiple layers, including bond wires, semiconductor dies, die attach, insulating substrates, baseplate solder and the baseplate itself.

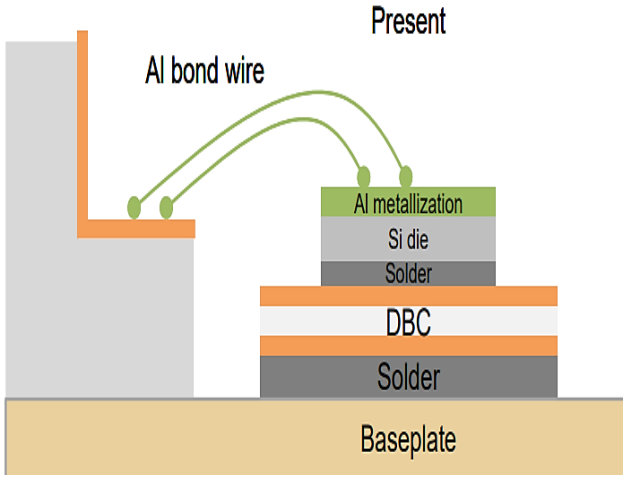

Fig. 3. Present power device structure with Al bond wires.

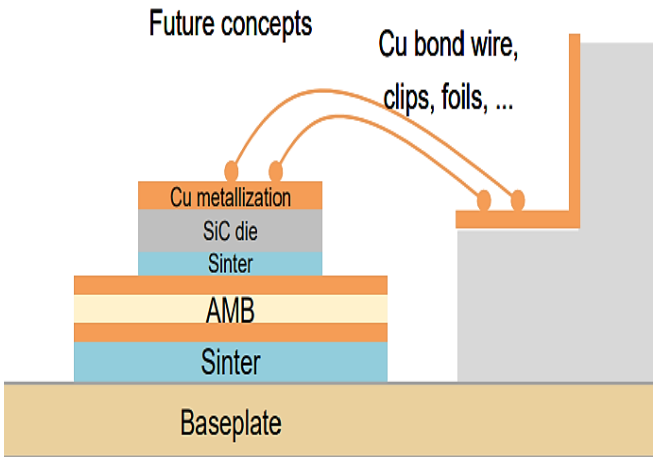

Fig. 4. Future power device structure with Cu bond wires and AMB substrate.

Each layer contributes to device performance but is also susceptible to various failure mechanisms. The power module industry is expected to transition towards WBG devices and advanced packaging technologies in the near future. These technologies include gallium nitride (GaN) and silicon carbide (SiC), copper bond wires, copper metallization, metal sintering, and active metal brazed (AMB) substrates etc. A possible future concept integrating these advanced packaging technologies is shown in Figure 4.

III. Low-Power DFT Optimization Techniques

Low-power Design-for-Test (DFT) optimization techniques aim to minimize test power while maintaining fault coverage and test time [13]. These techniques modify the DFT infrastructure or enhance the DFT infrastructure to restrict the number of switching actions that happen when the test applications are carried out. Scanning chain partitioning, clock gating, test point insertion, adaptive power scaling, and low-power test controllers are a few examples [14]. The techniques tend to be test-compression friendly and the industry is seeing a lot of the employment of these techniques so that one is able to carry out reliable power-aware testing at the use of appropriate controllers within the data-rates or in simple term, power-aware testing at the top of their semiconductor areas of manufacturing process.

A. Scan Chain Optimization

A set of n scan registers cc, along with a primary input port PI and a primary output port PO, make up a scan chain instance S= (R. PI, PO). The scan-in pin location in the is plane and the scan-oul pin location in the of plane are distinct for each register c_j. There is just one input position i_{n+1} and one output location on for PI and PO, respectively. A scan-out pin must connect to a scan-in pin at every edge of the scan chain. Altogether, it has the ability to access the scan registers as well as the PI and PO of S cells. D can stand for the distance matrix between cells; specifically, $D[i][j]$ is equal to the Manhattan distance between the scan-out pin of cell $c_i$and the scan-in pin of cell c_j. The cost of a scan chain is the total of distances between consecutive cells in the chain [15]. A scan chain for S is an ordering of the cells in S with PI at the beginning and PO at the end. S must be located along the most cost-effective chain in order to solve the scan chain ordering problem.

B. Test Data Compression

The goal of test data compression is to reduce the quantity of test data kept on the tester, including both stimulus and response data. The data volume and tester channel needs can be reduced using the compression techniques indicated in Figure 5 of (A - Decompressor, B - Compactor), which is a generic design:

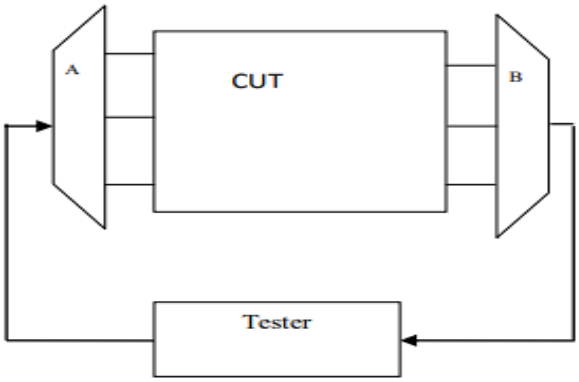

Fig. 5. Generic Architecture for Test Compression

The decompressor takes the compressed test vector as input from the tester, expands it and sends the expanded test vectors to the CUT. A small signature can be generated from a lengthy output response sequence by using the output compactor [16]. This supplementary hardware on-chip enables the compression of the test data. The three main types of test data compression algorithms are code-based, Broadcast-scan-based, and linear decompression-based, which are determined by the decompression hardware implementation.

C. Evolution of DFT with Technology Scaling and SoC Complexity

Technology scaling has also significantly influenced Design-for-Test (DFT) methodologies by introducing new complexities and requirements at advanced process nodes. As process nodes decline to 5nm and below, fault models must become more complex to include subtle physical defects, such as bridging faults, resistive opens, and even more complex layout-dependent anomalies [17]. Power gating and clock gating are examples of low-power design strategies that bring new challenges like untestable routes and erroneous fault detection. As a result, power-aware DFT insertion and validation are essential [18]. Additionally, the DFT challenges of multi-voltage domains and dynamic frequency scaling necessitate DFT solutions that vary and meet industry requirements across different conditions. At the same time, have minimum coverage and minimum overhead. As the integration of CPUs, GPUs, accelerators, and memory moves toward heterogeneous integration, which involves components on a single die or chipset, the necessity for modularity and hierarchy in DFT has been emphasized.

IV. Built-in Self-Test (BIST) and Low-Power Designs for Test DFT

Built-In Self-Test (BIST) is a feature that most DFTs include, and it lets circuits check their own functionality (on-chip test pattern development and response analyzing). BIST is also required to be power-efficient in modern low-power designs, in addition to reducing dependency on external test equipment and making testing convenient for users by providing access to it [19]. Since a large number of versions

of the BIST architecture can provide control over switching activity, they also have the potential for very high dynamic power consumption during self-test. Therefore, low-power BIST techniques must be developed that comprise gated clock modes, test pattern throttling, and weighted pseudo-random pattern generation. More power-sensitive types of logic will be used, especially in advanced BIST controllers to drive control of the timing and even the distribution of the test vectors. Due to these optimizations, BIST can continue to effectively find faults with relatively low energy consumption, making it suitable for portable and battery-powered semiconductor applications.

A. Proposed BIST Architecture with Modified Components

Figure 6 shows the use of a clock signal with a period of 1 ns and a Tonne (pulse width) of 0.05 ns, operating within a 1V range. The required 5-bit test vectors are generated by the suggested pattern generator using the clock pulse as an input [20]. The updated memory unit and the circuit under test (CUT) both take input from these 5-bit patterns. After that, we'll use the response analyzer to compare the CUT's (Circuit Under Test) output with the updated memory unit's output. If everything is working as it should, the result_x and result_y simulation curves in Figure 7 should stay at 1 V.

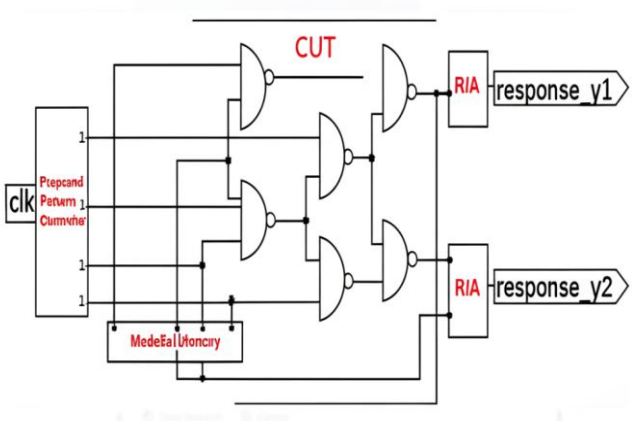

Fig. 6. Full BIST Architecture with modified components

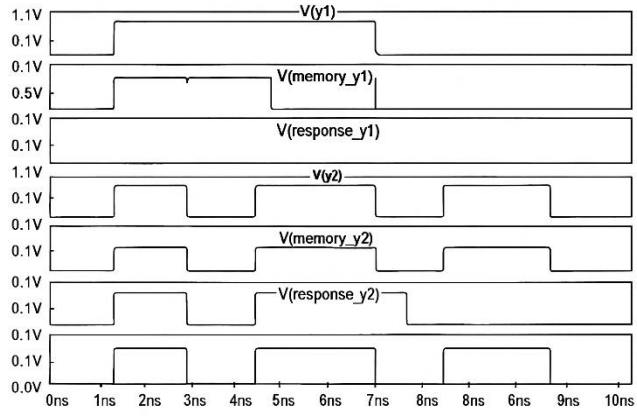

Fig. 7. Simulation plot for BIST Architecture

B. Power-Aware BIST Control Techniques

Built-in hardware features are utilized to achieve testing in the BIST design-for-test technique [21]. The BIST technique involves adding more circuits to the chip so it can test itself. When applied to VLSI testing, these methods significantly lessen both its difficulty and complexity [22]. Testing ensures that the design function and fabrication process are accurate. In addition, testing can be applied towards the end of a product's lifespan to identify defects brought on by wear and tear or environmental variables.

The methods used by BIST in memory can be categorized as:

- **On-line BIST:** Online BIST testing is possible even when the system is in its most typical operational state. Testing in this manner requires less time and occupies very little space. Once again,
- **Off-line BIST:** Outside of the internet. One method of testing that takes place when the system is not being used as it normally would is known as BIST. There is no area overhead for this testing, but it takes more time.

C. Low-Power Design Techniques

An integrated low-power approach necessitates optimization at each level of design abstraction, as shown below:

- **System:** Sectionalizing, Power reduction.
- **Algorithm:** Design complexity, operational concurrency, and operational regularity.
- **Architecture:** Data redundancy, process pipelines, and parallelism of operations, Coding and decoding of data
- **Circuit Logic:** Different approaches to logic design, energy recovery techniques, and component sizes.
- **Technology:** Capability to Lower Thresholds, Multiple Threshold Devices.

BIST enables circuits to test themselves using on-chip pattern generation and response analysis, reducing reliance on external equipment. However, conventional BIST can cause high dynamic power consumption. To address this, low-power BIST techniques such as clock gating, pattern throttling, and weighted pseudo-random generation are used. Modified BIST architectures improve efficiency and fault detection with minimal energy use, making them suitable for portable devices. BIST can be implemented as on-line (during operation) or off-line (during idle states). Low-power design further requires multi-level optimization across system, algorithm, architecture, logic, and technology layers.

V. Literature Review

This literature section provides a comprehensive overview of recent advancements in low-power semiconductor design and testing, emphasizing optimization techniques, power-aware test strategies, and emerging challenges across microprocessor design, memory BIST, VLSI methodologies, and ultra-low power scan testing solutions.

Rajavel (2025) explores the challenge of enhancing the efficiency of testing system-on-chip (SoC) semiconductor systems, which encompass heterogeneous computing cores and artificial intelligence (AI) accelerators. offer an examination of system-on-chip (SoC) design and current Design for Testability (DFT) approaches, taking into account power gating, clock gating, and dynamic voltage and frequency scaling (DVFS) as methods to reduce power consumption. Integrating low-power approaches into DFT can dramatically reduce energy usage (by an average of 20-35% without reducing test coverage quality), as shown by practical examples such as Qualcomm Snapdragon, Apple A-Series, and Tesla FSD. Combining power management methods with

standard scan chains, built-in self-test (BIST), and boundary scan effectively reduces thermal loads and increases reliability of modern systems on a chip (SoC) in mass manufacturing, according to the proposed analysis [23].

Zhang et al. (2024) Low-power microprocessor design and optimization techniques, focusing on how to effectively reduce power consumption without significantly affecting performance. they begin with an overview of the fundamentals and major challenges of low-power design, followed by an in-depth analysis of a variety of optimization techniques at the architectural level, circuit level, and algorithmic and software levels. the effects and tradeoffs of these techniques in practical applications through specific case studies, and provides an outlook on future trends and research directions in low-power microprocessor design. It provides a theoretical foundation and practical guidance for realizing more efficient and energy-saving microprocessor design, which has important academic value and application prospects [24].

Au et al. (2024) a stack of tools designed to keep tabs on memory instances and their linked Memory Built-In Self-Test (MBIST) devices' power consumption. The second part of the paper is devoted to the optimization of the memory test scheduling for a commercially available Design-for-Test (DFT) tool. System-on-Chip (SoC) memory testing causes increased power dissipation due to factors such as power supply voltage and technology node size. Methods that are less systematic, such as arranging memory tests manually, should be changed [25].

Deshpande et al. (2023) significance of semiconductor testing has grown much more. Mistakes or flaws in the chips, no matter how small, can lead to dangerous scenarios, costly product recalls, and damaged reputations. To ensure that semiconductors are free of flaws, engineers employ a battery of tests, including functional, structural, parametric, and reliability testing. The former determines how well an IC performs in its most fundamental roles, while the latter determines how long it will last in different environments. Electronic gadgets can only incorporate high-quality and reliable ICs if they undergo thorough semiconductor testing. This is crucial in order to meet the increasing demand for electronic devices in industries such as communication, healthcare, transportation, and aerospace [26].

Karthik et al. (2023) a thorough introduction to low-power very large-scale integration (VLSI) design approaches for several types of power dissipation sources and circuits based on complementary metal oxide semiconductors (CMOS) and complementary metal oxide field-effect transistors (CNTFETs). As a VLSI circuit designer working with CMOS and CNTFET (Carbon Nano Tube Field Effect Transistors) technology, one of the main issues is power consumption. Power consumption has risen to the status of paramount importance due to the ever-increasing operating frequencies, better integration, and scaling [27].

Yu et al. (2022) A source measure unit is used as the excitation source and measuring instrument in the automatic test system for semiconductor devices, while a relay array is used as the signal switching device. A single relay from the array will be activated and linked to the test circuit while the remaining relays are left in the off position during testing of various units. When the relay switch is turned off, a leakage current ranging from nanoamperes to microamperes will be introduced due to the high impedance insulating resistance between the contacts. Reducing the leakage current inaccuracy caused by relay insulation resistance is important when utilizing the automatic test system for semiconductor devices, as their leakage current is typically between a few nA and a few μA [28].

Iwata et al. (2021) a scan testing approach that is demonstrated to be effective for ultra-low power devices. It splits one scan shift clock into several scan shift clocks per clock domain. Moreover, it changes the scan shift clock speed to cope with the inrush current. These clock controls are made possible by their own test clock controller ow power devices have become widely designed. Since the power supply design is based on the user operation, there is the possibility that it can malfunction in conventional scan testing on account of the excessive power consumption during scan testing [29].

Table I presents a comparative analysis of recent studies on low-power semiconductor devices, highlighting diverse testing and optimization approaches, key findings, challenges, and future directions in power-efficient design.

TABLE I. LITERATURE SUMMARY ON LOW-POWER SEMICONDUCTOR DEVICES

Author	Study On	Approach	Key Findings	Challenges	Future Directions
Rajavel (2025)	Improving energy efficiency in testing of SoC devices with AI accelerators	Examining system-on-a-chip designs and density-functional theory approaches; assessing power-saving methods such as clock gating, DVFS, and power gating.	Integrating low-power techniques into DFT (e.g., in Snapdragon, Apple A-Series, Tesla FSD) can reduce energy usage by 20–35% without compromising test quality	Lack of a unified framework for power-efficient testing; difficulty in maintaining coverage while reducing power	Develop comprehensive DFT frameworks with adaptive power management; incorporate AI to optimize energy-efficient test generation
Zhang et al. (2024)	Low-power microprocessor design	Multi-level optimization: architectural, circuit, algorithmic, software	Effective power reduction without major performance loss; practical case studies included	Trade-offs in optimization levels; implementation complexity	Future trends in energy-saving microprocessor architecture
Au et al. (2024)	MBIST power monitoring and test scheduling	Toolchain for memory power tracking; optimized scheduling algorithms	Improved memory test efficiency with reduced power consumption	High power dissipation in SoC memory tests at lower tech nodes	Replacing manual scheduling with systematic power-aware techniques
Deshpande et al. (2023)	Semiconductor device testing	Overview of test types: functional, structural, parametric, and reliability	Testing ensures high IC quality across industries (healthcare, automotive, aerospace, etc.)	Managing diverse test types and ensuring consistency under varying use conditions	Advanced, scalable testing strategies to support growing IC complexity
Karthik et al. (2023)	Low-power VLSI design (CMOS & CNTFET)	Survey of power dissipation sources and reduction techniques	CNTFET and CMOS scaling demand advanced low-power methodologies	Increasing integration and frequency raise power and thermal concerns	Development of novel materials and scalable low-power architectures

Yu et al. (2022)	Automatic semiconductor test systems	Relay-based switching to minimize leakage current error	Relay insulation resistance introduces measurable leakage; must be addressed in auto-test systems	Leakage current error due to relay insulation; affects precision in low-current measurements	Enhanced isolation techniques and test system accuracy improvements
Iwata et al. (2021)	Scan testing for ultra-low power devices	Modified scan shift clock and domain-specific test clock controller	Reduces scan test power by distributing clock domains and controlling inrush current	Traditional scan testing causes excessive power in ultra-low power designs	Smarter test clock control for future ultra-low power ICs

VI. Conclusion and Future Work

The increasing complexity of modern semiconductor devices, along with rising demands for low-power, high-performance operation, has made Design-for-Test (DFT) essential in VLSI design. This review examined key low-power DFT techniques, including scan chain optimization, clock gating, test compression, and power-efficient Built-In Self-Test (BIST) architectures. As technology nodes scale down to 5nm and beyond, challenges such as excessive switching activity, leakage currents, and IR drops become more prominent, affecting test reliability and yield. DFT strategies must now account for multi-voltage domains, dynamic frequency scaling, and heterogeneous integration of CPUs, GPUs, and memory. Modular and hierarchical DFT frameworks have emerged to address these complexities, while low-power controllers and adaptive test methods help ensure efficiency. With its increasing application in portable electronics, automotive, and AI-driven systems, power-aware DFT is crucial for ensuring robust and energy-efficient testing. However, many techniques still struggle with scalability in advanced nodes.

Future research should focus on enhancing power-aware DFT methodologies to meet the demands of sub-5nm technology and complex heterogeneous SoC architectures. There is a need for smarter test pattern generation that adapts dynamically to real-time power budgets and workload conditions. The integration of AI-based test optimization and fault prediction can further enhance efficiency.

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